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10/799,783	03/12/2004	Jin-Kyoung Jung	SAM-0529	8323

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EXAMINER	
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2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,783	JUNG ET AL.	
	Examiner	Art Unit	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-12,14-23 and 25-44* is/are pending in the application.

4a) Of the above claim(s) *2,17-22 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-12,14-16,23,25-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004 and 18 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendments filed 5/11/2007 have been received and entered in the case.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3, 9, 30-32, 34-35,37, 40, 42 and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Rhee et al. (US 6774712).

With respect to claim 1, Figure 4 of Rhee discloses a semiconductor device, comprising: a control signal generating circuit (outputting PDPDEB) for generating a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits; and an internal voltage generating circuit (61) coupled to the control signal (PDPDEB), the internal voltage generating circuit comprising: a comparing circuit (51) for comparing a

reference voltage (output from 41) to an internal voltage (IVC) to generate a driving signal (output at 60) when the control signal is inactivated, wherein the comparing circuit comprises: a comparator (52) connected between a first node and a ground voltage and comparing the reference voltage to the internal voltage to generate the driving signal; and a switching circuit (58) connected between an external power voltage (+) applied to the comparator when the control signal is activated; a driving signal control circuit (60) for inactivating the driving signal when the control signal is activated; and an internal voltage driving circuit (53) for receiving the external power voltage (+) and generating the internal voltage in response to the driving signal.

With respect to claim 3, figure 4 discloses the device of claim 1, wherein the internal voltage driving circuit (54) includes a PMOS transistor which has a source to which the external power voltage (+) is applied, a gate to which the driving signal is applied, and a drain connected to an internal voltage generating terminal for generating the internal voltage (IVC) wherein the PMOS transistor turns the internal voltage to a reference voltage level in response to the driving signal and turns the internal voltage to a external power voltage level when the driving signal is inactivated.

With respect to claim 9, an input signal is not a structural component, because a signal has no structure. Furthermore, this operation is inherent in any transistor because an input signal changes the mode between either saturation, active, triode and cutoff modes. The limitation of a plurality of bits is suggested at least in the function of turning on which requires a low bit to high bit operation and encompasses at least two

bits. This limitation is also intended use because an input signal can be used in any device.

With respect to claims 30-32, these claims are deemed to be intended use. (Note: any value or number of bits input would correspond to the number of bits processed by the semiconductor because the input and the value of the bits have a causal effect on the semiconductor.) Also an input signal can be used in any device.

With respect to claims 34-35 and 37 are rejected for similar reasons as above.

With respect to claims 40, 42 and 44 the PMOS device or the NMOS device meet the claimed limitation because they are activated when at least a single bit in input. Furthermore these claim limitations are deemed inherent since the claimed structure is fully anticipated by Rhee et al.

With respect to claims 41, 43 and 39 these claim limitations are deemed inherent since the claimed structure is fully anticipated by Rhee et al.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee et al. (US 6774712) in view of Sher.

With respect to claim 7-8, figure 4 of Rhee discloses the device of claim 1 but fails to disclose wherein the control signal generating circuit comprises a fuse to generate the control signal responsive to the input signal. Figure 1 and 18 of Sher teach using a bond pad with a fuse to generate an input signal. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the bond pad and the fuse in Sher in the control signal generating circuit of Rhee for the purpose of protecting the control signal generating circuit from an high current.

6. Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee et al. (US 6774712)in view of Bae et al. (US 6373754).

With respect to claim 2, figure 4 teaches the device of claim 1, wherein the driving signal control circuit includes a transistor which has a drain connected to a driving signal generating terminal for generating the driving signal, a gate to which the control signal is applied and a source connected to a voltage. Bae et al. teaches the use of an NMOS or a PMOS interchangeable to control the driving signal. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a NMOS instead of a PMOS as the driving signal control circuit, for the purpose changing the activation signal.

7. Claims 33, 36 and 38 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee et al. in view of Park et al.(US 5349559)

With respect to claims 33, 36 and 38, figure 4 of Rhee et al. discloses the circuit above, but fails to disclose wherein the circuit comprises a second switching device. Figure 4 of Park et al teaches the use of a dual transistor CMOS switch to drive a internal control signal. It would have been obvious at the time the invention was made to a person having ordinary skill in the art, to use any switch to the driving of the internal voltage driving signal circuit, for the purpose of stability in the switching process.

8. Claims 10-12, 14-17, 23, 25 and 27-29 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki (20020053943) in view of Sher (US 6633196).

With respect to claim 10, figure 1 and 5a of Yamasaki discloses a semiconductor device comprising; a control signal generating circuit (5a) for generating a control signal (TE) responsive to an input signal (/RAS, /CAS, /WE or Add) related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits; and an internal voltage generating circuit (Figure 1) coupled to the control signal generating circuit for receiving the control signal (TE), the internal voltage generating circuit comprising a comparing circuit (CMP) for comparing a reference voltage (Vref) to an internal voltage (IntVcc) to generate a comparing signal; a switching circuit (DR)

coupled (to connect for consideration together) to both the control signal generating circuit (3) and an output of the comparing circuit (CMP) for receiving the control signal transmitting the comparing signal as a driving signal when the control signal (TE) is inactivated and a driving signal control circuit (2) for inactivating the driving signal when the control signal is activated and an internal voltage driving circuit (RFG, Figure 20) for receiving an external power voltage (EX) and generating the internal voltage in response to the driving signal but fails to disclose wherein the switching circuit includes a CMOS transmission gate which transmits the comparing signal as the driving signal when the control signal is inactivated. Figures 3a and 3b of Sher teaches the use of CMOS transmission gates for NMOS transistor switching elements. It would have been obvious at the time the invention was made to one of ordinary skill in the art to substitute the NMOS switching elements of Yamasaki with CMOS transmission gates for the purpose of improving switching speed.

With respect to claim 11, the above circuit produces the circuit of claim 10 wherein the driving signal control circuit includes an NMOS transistor (2f) which has a drain connected to the driving signal generating terminal (via 2ba) for generating the driving signal, a gate to which the control signal (TE) is applied, and a source connected to a ground voltage.

With respect to claim 12, the above circuit produces the circuit of claim 10 wherein the internal voltage driving circuit includes a PMOS transistor (DR) which has a source to which the external power voltage is applied (EX) a gate to which the driving signal is applied, and a drain connected to an internal voltage generating terminal for generating

the internal voltage (IntVcc) wherein the PMOS transistor turns the internal voltage to a reference voltage level in response to the driving signal and turns the internal voltage to an external power voltage when the driving signal is inactivated.

With respect to claim 14, the above circuit produces the circuit of claim 10 but fails to produce the control signal generating circuit wherein the input signal is generated using a fuse. It is well known in the art to use a laser burned fuse to generate an irreversible signal that can be controlled externally. It would have been obvious at the time the invention was made to one of ordinary skill in the art to use a fuse to generate an input signal for the purpose of making the input signal irreversible.

With respect to claim 15, the recitation of the control signal generating circuit comprising an external pad to generate the control signal responsive to the input signal is deemed to be inherent because in a semiconductor device an external pad is inherently used to connect to circuits.

With respect to claim 16, the circuit above produces the circuit of claim 23, wherein the control signal generating circuit (5a) activates or inactivates the control signal by receiving a mode setting signal together with a mode setting command. (See paragraphs [0093] and [0094]).

With respect to claim 23, figure 1 and 5a of Yamasaki discloses a control signal generating circuit (5a) for generating a control signal (TE) responsive to an input signal (/RAS, /CAS, /WE or Add) related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is

more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits; and an internal voltage generating circuit (Figure 1) coupled to the control signal generating circuit for receiving the control signal (TE) and comparing a reference voltage (Vref) to an internal voltage (IntVcc) to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, and to make the internal voltage have an external power voltage level when the control signal is activated, wherein the internal voltage generating circuit comprises at least one of a first switching circuit (2e) that cuts off an external power voltage applied to the internal voltage generating circuit when the control signal (TE) is activated, a second switching circuit (2f) that cuts off a ground voltage supplied to the internal voltage generating circuit when the control signal (TE) is activated and a third switching circuit (2c) but fails to disclose the third switching circuit including a CMOS transmission gate which transmits the driving signal when the control signal is inactivated. Figures 3a and 3b of Sher teaches the use of CMOS transmission gates for NMOS transistor switching elements. It would have been obvious at the time the invention was made to one of ordinary skill in the art to substitute the NMOS switching elements of Yamasaki with CMOS transmission gates for the purpose of improving switching speed.

With respect to 25, the circuit above produces the circuit of claim 23, wherein the internal voltage generating circuit includes a comparing circuit (CMP) for comparing the reference voltage to the internal voltage (IntVcc) to generate a comparing signal; the

third switching circuit (DR) for transmitting the comparing signal as a driving signal when the control signal is control signal is inactivated; a driving signal control circuit (2) for inactivating the driving signal when the control signal is activated and an internal voltage driving circuit (RFG, Figure 20) for receiving an external power voltage (EX) and generating the internal voltage in response to the driving signal.

With respect to claim 27, the above circuit produces the circuit of claim 23 but fails to produce the circuit wherein control generating circuit comprises a fuse to generate the control signal responsive to the input signal. It is well known in the art to use a laser burned fuse to generate an irreversible signal that can be controlled externally. It would have been obvious at the time the invention was made to one of ordinary skill in the art to use a fuse to generate an input signal (in the control signal generating circuit) for the purpose of making the input signal irreversible.

With respect to claim 28, the recitation of the control signal generating circuit comprises an external pad to generate the control signal responsive to the input signal is deemed to be inherent because in a semiconductor device an external pad is inherently used to connect to circuits.

With respect to claim 29, the circuit above produces the circuit of claim 23, wherein the control signal generating circuit (5a) activates or inactivates the control signal by receiving a mode setting signal together with a mode setting command. (See paragraphs [0093] and [0094]).

Response to Arguments

9. Applicant's arguments filed 5/11/2007 have been fully considered but they are not persuasive.

With respect to applicant's argument "Rhee et al. fails to teach or suggest a control signal generating circuit for generating a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the nmber of data bits being processed by the semiconductor device is more than a predetermined number of bits and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits", the Examiner disagrees. A change from a low to high or a high to low can be considered a bit. A control signal is inherent in a transistor because a transistor acts as a switch and must be controlled at the input of the gate or base. A predetermined number of bits is also inherent. Whether a transistor is a p or n enhancement or depletion transistor if a bit is greater than a threshold the transistor is activated. Similarly if a bit is less than a threshold the transistor is activated. The predetermined number of bits can be zero, because zero is a number. If there is a change in the threshold of the voltage to be considered a bit the transistor shifts from on to off or off to on when a bit is present.

With respect to applicant's argument that Rhee fails to teach or suggest a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when a control signal is inactivated, wherein the comparing circuit

comprises a comparator connected between a first node and a ground voltage and comparing a reference voltage to an internal voltage to generate the driving signal and a switching circuit connected between an external power voltage and the first node and cutting off the external power voltage applied to the comparator when the control signal is activated as claimed in independent claim 1, the Examiner disagrees. Where any to circuits are connected or directly connected there is a node (a junction between interconnected circuits). Specifically the first node is referring to the node between circuits 58 and 52 (but can be other nodes). The figure 4 of Rhee clearly shows that comparator 52 is also connected (attached so as to influence) through several direct paths, one of the paths being via (46, 48 and 50) to ground. The external power source is connected to 58 at the source and the first node is at the drain. Thus the reference in figure 4 reads on the claim.

With respect to claim 9, an input signal is not a structural component, because a signal has no structure. Furthermore, this operation is inherent in any transistor because an input signal changes the mode between either saturation, active, triode and cutoff modes. The limitation of a plurality of bits is suggested at least in the function of turning on which requires a low bit to high bit operation and encompasses at least two bits.

With respect to applicant's argument the Rhee et al. fails to teach or suggest a control signal generating circuit for generating a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of

data bits being processed by the semiconductor device is more than a predetermined number of bits and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits as claimed in independent claim 34, the Examiner disagrees. Again, this claim is inherent in the operation of any transistor because a transistor is designed to operate in such a manner that it is activated when an input signal indicated that a bit (or control signal) is past a certain threshold.

With respect to applicant's argument that Rhee et al. fails to teach or suggest a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated, wherein the comparing circuit comprises a comparator connected between the external power voltage and a first node and comparing the reference voltage to the internal voltage to generate the driving signal, and a switching circuit connected between the first node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated, the Examiner disagrees. The comparing circuit is 52, which compares an internal voltage coming from 56 to a reference voltage coming from 44 to generate a driving signal coming from 58 when the control signal is inactivated (i.e. low). The external power voltage is coming into the source of 58 and the first node is between 58 and 52. The ground voltage is cut off when PDPDE is not activated (i.e low).

With respect to applicant's argument that Rhee et al. fails to teach or suggest a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated, wherein the comparing circuit

includes a comparator connected between a first node and a ground voltage and comparing the references voltage to the internal voltage to generate the driving signal and a switching circuit connected between he external power voltage and the first node cutting off the external power voltage applied to the comparator when the control signal is activated, the examiner disagrees for reasons as above.

With respect to applicant's arguments concerning claim 37, the Examiner disagrees for similar reasons as above.

With respect to applicant's arguments concerning Bae et al. and Park, the Examiner disagrees. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

With respect to applicant's argument that neither Yamasaki nor Sher suggests a control signal generating circuit for generating a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated whenthe input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits being processed by the semiconductor device is less than the predetermined number of bits as claimed in independent claim 10, the examiner disagrees. This limitation is inherent in the functionality of the system. The rise and fall during the test mode and the signal is inactivated and activated during the test mode, this is sufficient to meet the claim language because the predetermined number of bits

can be 0. Furthermore the VDC is coupled (to connect for consideration together) to circuit 3 via 2c,

With respect to applicant's argument circuit 2 of Yamasaki et al. does not comprise a comparing circuit for comparing a reference voltage to an internal voltage to generate a comparing signal as claim 1, the Examiner disagrees. Vrfo is internal to the circuit and therefore is an internal voltage. Differential amplifier 2b is a comparing circuit because it compares a reference voltage to another voltage input (i.e. Vrfo)

With respect to applicant's argument there is not teaching or suggestion of either the VDC or the driving circuit 2 including a switching circuit coupled (to connect for consideration together) to both a control signal generating circuit and an output of a comparing circuit for receiving a control signal and for transmitting a comparing signal as a driving signal when the control signal is inactivated, wherein the switching circuit includes a CMOS transmission gate which transmits comparing signal as the driving signal when the control signal is inactivated, the Examiner disagrees. DR receives a control signal from the comparator (CMP) and transmits EX to the comparator driving CMP when it is inactivated (i.e has a low input).

With respect to applicant's further arguments concerning Yamasaki and Sher, the Examiner disagrees. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KEA
8/3/2007

Quan.Tra
Primary Examiner